

Spray-combustion synthesis: Efficient solution route to high-performance oxide transistors

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Metal-oxide (MO) semiconductors have emerged as enabling materials for next generation thin-film electronics owing to their high carrier mobilities, even in the amorphous state, large-area uniformity, low cost, and optical transparency, which are applicable to flat-panel displays, flexible circuitry, and photovoltaic cells. Impressive progress in solution-processed MO electronics has been achieved using methodologies such as sol gel, deep-UV irradiation, preformed nanostructures, and combustion synthesis. Nevertheless, because of incomplete lattice condensation and film densification, high-quality solution-processed MO films having technologically relevant thicknesses achievable in a single step have yet to be shown. Here, we report a low-temperature, thickness-controlled coating process to create high-performance, solution-processed MO electronics: spray-combustion synthesis (SCS). We also report for the first time, to our knowledge, indium-gallium-zinc-oxide (IGZO) transistors having densification, nanoporosity, electron mobility, trap densities, bias stability, and film transport approaching those of sputtered films and compatible with conventional fabrication (FAB) operations.

oxide transistor | low-temperature growth | combustion synthesis | transistor | oxide film

Metal-oxide (MO) semiconductors, especially in amorphous phases, represent an appealing materials family for next generation electronics owing to their high carrier mobilities, good environmental/thermal stability, mechanical flexibility, and excellent optical transparency (1–3). MO films complement organic semiconductors (4, 5), carbon/oxide nanomaterials (6), and flexible silicon (7, 8) for enabling new technologies, such as flexible displays and printed sensors. For fabricating high-performance electronics with acceptable fidelity, conventional processes require capital-intensive physical/chemical vapor deposition techniques. Capitalizing on the solubility of MO precursors in common solvents, solution methods have been used to fabricate semiconducting MO layers for thin-film transistors (TFTs). However, the fabrication process and field-effect mobilities of these TFTs are not competitive with the corresponding vapor-deposited (e.g., sputtered) devices (9), and developing routes to solution-derived MO TFTs with technologically relevant thicknesses and performance comparable to state of the art vapor-deposited devices is a critical milestone for MO electronics evolution.

Sol-gel techniques are used extensively for MO film growth, including films for high-performance TFTs (10–13). However, the required sol-gel condensation, densification, and impurity removal steps typically require >400–500 °C processing temperatures, which are incompatible with inexpensive glasses and typical flexible plastic substrates (14). Progress toward significantly reducing the processing temperatures of sol gel-derived MO films has afforded excellent TFT mobilities; however, achieving both reproducible high-performance and stable device operation remains an unsolved issue for Ga-containing materials (15). Sol-gel on-a-chip for indium-zinc-oxide (3) and deep-UV irradiation of spin-coated

MO precursor films (1) represent significant advances; however, challenges remain. Recently, this laboratory reported a low-temperature solution method, spin-coating combustion synthesis (spin-CS), for fabricating MO TFTs (*SI Appendix, Fig. S1*) (2, 16). By incorporating an oxidizer and a fuel in the precursor solution, localized, highly exothermic chemical transformations occur within the spin-coated films, effecting rapid condensation and M-O-M lattice formation at temperatures as low as 200–300 °C, which was assessed by thermal and X-ray diffraction (XRD) analysis, and yielding high-performance TFTs. Additional work has subsequently broadened the spin-CS fuel/oxidizer options and accessible MO compositions (17).

Note, however, that independent of the particular solution processing method, significant quantities of gaseous H₂O, N₂, NO_x, CO₂, etc. are evolved, compromising film continuity and densification in single-step, thick-film growth processes (17–21). These issues also apply to combustion synthesis, especially because the exotherm is of short duration. Therefore, films must be sufficiently thin (typically <10–20 nm for conventional sol gel and <5–10 nm for combustion) to yield high-quality films (2, 3, 15). For MO TFT implementation in, for example, active-matrix display backplanes, semiconductor thicknesses must be 50–100 nm to avoid back-channel effects, delayed turn-on, and bias stress shifting (22, 23). Thus, for current generation MO TFT structures, suitable film thicknesses from conventional solution processes require inefficient multiple deposition and anneal sequences, which are time-consuming, and invariably create bulk trap states at the semiconductor interfaces.

Significance

Although impressive progress in solution-processed metal-oxide (MO) electronics has been achieved, fundamental science challenges remain concerning whether solution-processed MO materials and particularly technologically relevant, indium-gallium-tin-oxide (IGZO), can achieve efficient and stable charge transport characteristics when processed at low temperatures for short times and how IGZO film density, porosity, carrier mobility, and charge trapping can be manipulated. Here, we report a coating technique, spray-combustion synthesis, and demonstrate IGZO semiconductor thickness, densification, nanoporosity, electron mobility, trap densities, and bias stress stability approaching the quality of sputtered films.

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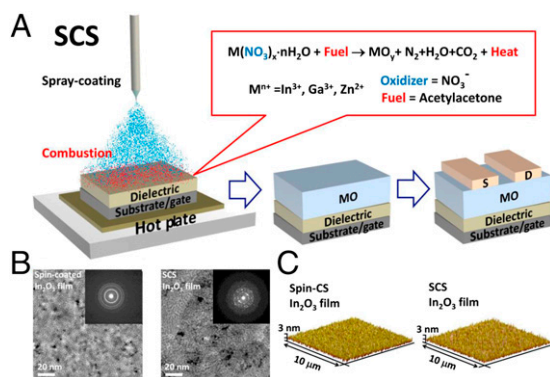


Fig. 1. SCS of MO films and corresponding morphological characterization. (A) Schematic of the SCS process used for growing MO films under ambient conditions and the corresponding bottom gate top contact TFT structure used in this study. (Inset) Combustion reaction for a generic metal nitrate acting as the oxidizer and acetylacetone as the fuel. (B) High-resolution, bright-field transmission electron microscopy (TEM) images and (insets) selected area energy-filtered electron diffraction patterns of In_2O_3 films deposited by spin coating and SCS. (C) Atomic force microscopy images of 20-nm In_2O_3 films.

In contrast to spin coating, spray processes are readily adapted to continuous large-area, high-throughput coating as in roll-to-roll processing. Simple spray coating has been used to fabricate organic solar cells (24), organic TFTs (25), and MO electronics (26) using heated substrates. In pioneering work, spray-coated sol-gel ZnO TFTs achieved mobilities of $\sim 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for 200 °C growth and $\sim 25 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for 500 °C growth (26). These results raise the intriguing question of whether combustion processing can be combined with spray coating to realize, at low temperatures, dense high-mobility MO films having significant, precisely controlled thicknesses in a single step and specifically, growing the most technologically relevant oxide film materials: semiconducting indium-gallium-tin oxide (IGZO) and conducting indium-tin-oxide (ITO).

Here, we report a low-temperature, nanometer-thickness, controlled solution route to high-performance MO electronics through spray-combustion synthesis (SCS). Reduced gaseous byproduct trapping yields dense, high-quality, macroscopically continuous films of both crystalline and amorphous MOs. Single-layer (50-nm-thick) IGZO TFTs with carrier mobilities 10^2 – $10^4 \times$ greater (7–20 cm^2/Vs) than those achieved with sol gel and conventional combustion synthesis are demonstrated and rival those of magnetron-sputtered IGZO TFTs. Film characterization includes the first positron annihilation spectroscopy (PAS) measurements on oxide thin films to our knowledge, X-ray photoelectron spectroscopy (XPS), X-ray reflectivity (XRR), and capacitance-voltage (C-V) data, supporting the broad applicability of SCS.

Results

MO Film Fabrication and Characterization. Fig. 1A and SI Appendix, Fig. S1 illustrate the SCS and spin-CS processes as well as the TFT structures. We first compare 20-nm-thick MO films fabricated in a conventional 4 × 5-nm spin-CS (four layers) or a single SCS step (one layer). Note that the time required for the former process (~ 100 min) is $\sim 12 \times$ the latter. To show broad SCS applicability, three different semiconductor MO film classes [In_2O_3 , indium zinc oxide (IZO), and IGZO] are grown at 200–300 °C on several substrates (Si/SiO₂, indium-tin-oxide/ZrO_x, AryLiteR/Al₂O₃, and glass). XRD analysis reveals that the SCS In_2O_3 films are polycrystalline and exhibit far stronger, sharper Bragg reflections than those fabricated by spin-CS, indicating enhanced film crystallinity (SI Appendix, Fig. S2). Not unexpectedly, 20-nm IZO and IGZO films grown at 200–300 °C by both methods are amorphous, consistent with reports that doping In_2O_3 with Zn^{2+} or Ga^{3+} frustrates crystallization (27–30). XPS oxygen 1s analysis of the O-bonding states in the films (SI Appendix, Fig. S3) indi-

cates three different oxygen environments: M-O-M lattice species at 529.9 ± 0.1 eV, bulk and surface metal hydroxide (M-OH) species at 531.3 ± 0.1 eV, and weakly bound adsorbate species (e.g., H₂O or CO₂) at 532.2 ± 0.1 eV (31–33). The In_2O_3 films in SI Appendix, Fig. S3 reveal the evolution of M-O-M characteristics with increasing processing temperatures and at the same annealing temperature, a higher density of M-O-M species in the SCS-derived In_2O_3 films vs. the spin-CS ones, which is in agreement with the film XRD data. Similar trends hold for SCS and spin-CS IZO and IGZO films (SI Appendix, Figs. S3 and S4). We attribute the microstructural and chemical properties of the SCS films to enhanced combustion efficiency promoting greater densification (vide infra). Bright-field TEM and selected area energy-filtered nanobeam diffraction images of SCS and spin-CS In_2O_3 films processed at 300 °C (Fig. 1B and B, Insets) indicate that the former are more crystalline than the latter, which is in agreement with the XRD data.

Semiconductor-layer morphology is critical for TFT performance, because it strongly affects interfacial trap density and electrical contacts (34–36). In previous spin-CS studies, very smooth surface topologies were achieved for thin (5-nm) single-layer/multilayer films ($\rho_{\text{RMS}} = 0.2$ – 0.5 nm) (2, 16). However, thicker (20- to 50-nm) single-layer films are significantly more porous and rougher ($\rho_{\text{RMS}} > 1$ nm) (2, 16), reminiscent of conventional thick sol-gel oxide films (17–21). In this work, atomic force microscopy and SEM images show that optimized single-layer SCS growth yields smooth thicker oxide films (Fig. 1C and SI Appendix, Figs. S5–S9). Thus, 20- and 50-nm-thick SCS-derived In_2O_3 , IZO, and IGZO films have $\rho_{\text{RMS}} < 0.6$ – 0.7 nm. Comparing scanning transmission microscope high-angle annular dark-field images, which are insensitive to diffraction and phase contrast, the pore size distribution of 20-nm polycrystalline In_2O_3 films fabricated by SCS (single layer) or spin-CS (multilayers), indicates smaller-sized porosity for the former (dark regions denote lower mass density areas than the surrounding light gray matrix in SI Appendix, Fig. S10). Thus, all morphology and porosity metrics indicate that the SCS films are denser and smoother.

MO TFT Performance. To investigate SCS generality for TFTs of diverse oxide semiconductors, spin-CS- and SCS-coated In_2O_3 , IZO (In:Zn = 1:0.43), and IGZO (In:Ga:Zn = 1:0.11:0.29) films were grown at various temperatures with 20-nm semiconductor films on p-doped silicon Si/300-nm SiO₂ substrates with 40-nm Al source/drain electrodes (50- μm channel length, 1.0-mm channel width). MO compositions were selected on the basis of previous studies indicating optimum mobility and gate modulation (37). Representative transfer and output plots and device statistics are shown in Fig. 2, Table 1, and SI Appendix, Figs. S11–S14. In_2O_3 TFTs can be processed at lower temperatures (200 °C) than the corresponding IZO and IGZO TFTs (225–300 °C) because of the differing Zn^{2+} and Ga^{3+} oxygen affinity vs. that of In^{3+} (14). Note that the SCS TFT performance is significantly greater than that of spin-CS devices for the same processing temperatures. Thus, the highest SCS In_2O_3 TFT mobility of $1.93 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ obtained at 200 °C is more than $2 \times$ greater than that of 200 °C spin-CS In_2O_3 devices. When annealing is increased to 300 °C, the SCS In_2O_3 TFT μ_{max} increases to $18.20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Similarly, the mobilities of 300 °C SCS IZO ($\mu_{\text{max}} = 9.47 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and IGZO ($\mu_{\text{max}} = 7.53 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) TFTs are also dramatically enhanced vs. the corresponding spin-CS devices ($\mu_{\text{max}} = 7.43 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for In_2O_3 , $\mu_{\text{max}} = 3.69 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for IZO, and $\mu_{\text{max}} = 3.65 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for IGZO), despite the $>10 \times$ reduction in MO film growth time. Furthermore, the linear mobilities are very similar to those obtained in saturation (SI Appendix, Fig. S14), consistent with the good current-voltage characteristics of our SCS devices. Furthermore, introducing a solution-processed high-dielectric constant (k) ZrO₂ dielectric increases the IZO SCS μ_{max} to $93.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with on/off $>10^5$ at low operating voltages of 2 V owing to the enhanced capacitance of the gate dielectric (Fig. 2 and SI Appendix, Fig. S13) (38). From these results, the SCS performance enhancement vs. spin-CS processing plausibly reflects more extensive M-O-M lattice

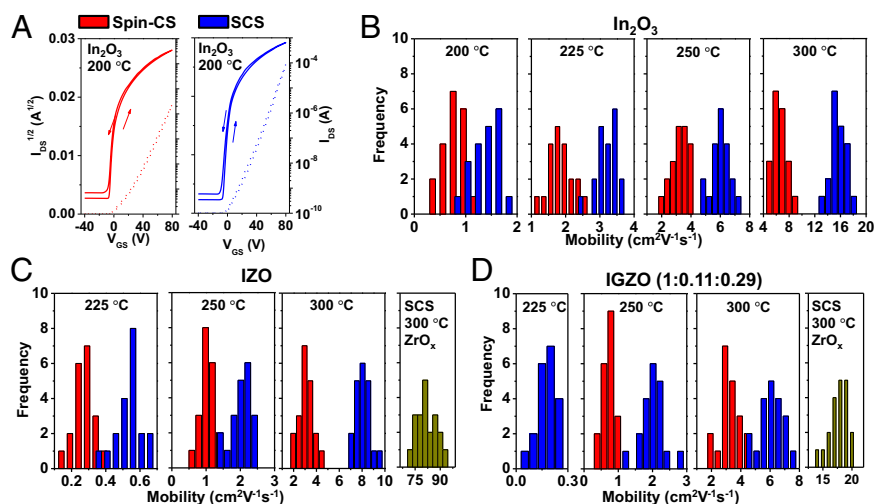


Fig. 2. Transistor transfer characteristics and mobility distribution statistics for 20-nm-thick MO TFTs fabricated on SiO₂/Si substrates (unless indicated otherwise) by spin-CS (four MO layers that are 5-nm thick) and SCS (single 20-nm MO layer). (A) Representative transfer plots ($V_D = 80$ V) for In₂O₃ devices annealed at 200 °C. (B) Corresponding saturation mobility distribution for In₂O₃ at the indicated temperatures. (C) Saturation mobility distribution for IZO (In:Zn = 1:0.43) at the indicated temperatures. Panel 4 refers to statistics for ZrOx/indium-tin-oxide (ITO) substrates. (D) Saturation mobility distribution for IGZO (In:Ga:Zn = 1:0.11:0.29) at the indicated temperatures. Panel 4 refers to statistics for ZrOx/ITO substrates.

densification and distortional relaxation, thereby reducing trap sites. Note also, in Table 1, that, despite the simple spray setup, the SCS-deposited TFT device metrics have significantly lower SDs (<15%), indicating greater TFT uniformity and hence, the greater reproducibility needed for large-scale fabrication (36). Finally, flexible In₂O₃ TFTs can also be fabricated by SCS at 200 °C on Arylite polyester [Arylite/Al(gate)/Al₂O₃/In₂O₃/Al(source/drain)] (*SI Appendix, Fig. S16*) and afford respectable performance: $\mu \sim 11$ cm² V⁻¹ s⁻¹, $V_T \sim +0.6$ V, $I_{on}/I_{off} \sim 10^4$.

Single-Layer IGZO Transistors. SCS growth of thicker, single-layer 50-nm IGZO films was next investigated, because this thickness is the minimum thickness required for IGZO TFT manufacture (39) and SCS significantly reduces device fabrication time. On a laboratory scale, 50-nm-thick IGZO films can be grown by SCS in ~20 min—comparable with typical sputtering times, excluding chamber evacuation—whereas multiple spin/annealing used in spin-CS and sol-gel IGZO coatings requires > 4 h, a process flow and time unacceptable for microelectronics. Thus, in a comparative study, TFTs with 50-nm-thick In:Ga:Zn = 1:0.11:0.29 IGZO films grown by one-step sol-gel spin coating, one-step spin-CS, and magnetron sputtering (target composition In:Ga:Zn = 1:1:1) were evaluated (Fig. 3 A and B and Table 2). The sol-gel TFT performance is poor ($\mu \sim 10^{-3}$ cm² V⁻¹ s⁻¹), because 300 °C/30-min annealing is inadequate for densification (17, 20). Reflecting the low combus-

tion efficiency of thicker films, the single-layer spin-CS IGZO TFTs also exhibit poor performance ($\mu \sim 10^{-2}$ cm² V⁻¹ s⁻¹) for 300 °C processing. In contrast, maximum mobilities of 7.6 cm² V⁻¹ s⁻¹ and $I_{on}/I_{off} \sim 10^8$ are obtained for SCS IGZO TFTs, $\sim 10^3$ – 10^4 × greater than for the sol-gel and spin-CS devices and approaching those of sputtered 1:1:1 IGZO devices ($\mu_{average} = 10.9$ cm² V⁻¹ s⁻¹, $\mu_{max} = 12.8$ cm² V⁻¹ s⁻¹, $I_{on}/I_{off} \sim 10^8$, $T_a = 300$ °C). The sputtered IGZO device metrics are typical values achieved in fabrication (FAB) lines using a 300-nm-thick SiOx layer. Note that IGZO TFTs fabricated by spray pyrolysis coating using the SCS metals composition but without fuel (spray) (Fig. 3B and *SI Appendix, Fig. S1*) perform poorly ($\mu_{average} = 0.53$ cm² V⁻¹ s⁻¹, $\mu_{max} = 0.71$ cm² V⁻¹ s⁻¹), showing that combustion synthesis is essential for achieving high-quality thick IGZO films by spray techniques at these temperatures. Finally, using a high-k ZrO₂ dielectric, SCS μ_{max} increases to 21.3 cm² V⁻¹ s⁻¹ with on/off $\sim 10^5$ at 2-V TFT operation (Fig. 3B).

Next, solution-processed IGZO films with In:Ga:Zn = 1:1:1 and annealing conditions (350 °C) identical to typical commercial sputtering protocols were investigated. This composition space is seldom studied for solution-processed IGZO TFTs, because large Ga contents degrade TFT function for processing at <500 °C. TFTs based on 50-nm-thick, sputtered sol-gel, spin-CS, and SCS IGZO films on Si/SiO₂ substrates were fabricated (Fig. 3 C and D and Table 2); not unexpectedly, the sol-gel and spin-CS devices perform poorly

Table 1. Performance metrics of 20-nm In₂O₃, IZO, and IGZO TFTs on 300-nm SiO₂/Si substrates with Al source/drain electrodes after various processing temperatures

MO	Spin-CS (4 × 5-nm MO) TFTs					SCS (20-nm MO) TFTs				
	T_a (°C)	Mobility (cm ² /Vs)	V_T (V)	V_{ON} (V)	I_{on}/I_{off}	T_a (°C)	Mobility (cm ² /Vs)	V_T (V)	V_{ON} (V)	I_{on}/I_{off}
In ₂ O ₃	200	0.83 ± 0.17	11.5 ± 5.1	-6.7 ± 4.8	$\sim 10^5$ – 10^6	200	1.44 ± 0.22	9.6 ± 5.0	-8.4 ± 5.1	$\sim 10^5$ – 10^6
In ₂ O ₃	225	1.87 ± 0.27	9.5 ± 3.7	-8.1 ± 4.2	$\sim 10^5$ – 10^6	225	3.15 ± 0.23	9.1 ± 5.2	-7.4 ± 4.5	$\sim 10^5$ – 10^6
In ₂ O ₃	250	3.24 ± 0.41	-2.3 ± 3.8	-18.3 ± 3.9	$\sim 10^4$ – 10^5	250	6.11 ± 0.49	-11.2 ± 5.8	-19.9 ± 4.9	$\sim 10^3$ – 10^4
In ₂ O ₃	300	6.57 ± 0.85	-16.1 ± 4.3	-27.8 ± 4.7	$\sim 10^3$ – 10^4	300	15.45 ± 1.03	-26.7 ± 5.4	-38.7 ± 5.0	$\sim 10^3$ – 10^4
IZO	225	0.29 ± 0.05	24.2 ± 4.1	3.8 ± 3.8	$\sim 10^6$ – 10^7	225	0.52 ± 0.06	20.2 ± 4.6	0.4 ± 4.4	$\sim 10^6$ – 10^7
IZO	250	0.95 ± 0.18	21.5 ± 3.8	1.3 ± 4.1	$\sim 10^6$ – 10^8	250	2.06 ± 0.26	17.5 ± 3.1	-2.6 ± 3.4	$\sim 10^6$ – 10^7
IZO	300	3.18 ± 0.51	9.3 ± 3.2	-10.8 ± 3.5	$\sim 10^6$ – 10^8	300	8.05 ± 0.53	9.8 ± 3.5	-8.1 ± 3.2	$\sim 10^6$ – 10^7
IZO*						300	81.5 ± 5.66	-0.28 ± 0.09	-0.72 ± 0.10	$\sim 10^4$ – 10^5
IGZO	225	0.01 ± 0.005	35.4 ± 9.1	24.6 ± 7.9	$\sim 10^5$ – 10^6	225	0.18 ± 0.05	30.3 ± 8.7	19.8 ± 7.6	$\sim 10^5$ – 10^6
IGZO	250	0.77 ± 0.14	22.6 ± 3.4	0.5 ± 3.1	$\sim 10^6$ – 10^8	250	1.97 ± 0.26	20.1 ± 3.5	-0.4 ± 3.3	$\sim 10^6$ – 10^7
IGZO	300	3.31 ± 0.54	20.1 ± 3.3	1.9 ± 3.4	10^8	300	6.34 ± 0.69	17.5 ± 3.2	-5.5 ± 3.5	$\sim 10^6$ – 10^7
IGZO* [†]						300	17.8 ± 1.34	0.11 ± 0.02	-0.35 ± 0.02	$\sim 10^4$ – 10^5

Average of ≥20 devices. Measured in ambient conditions: relative humidity (RH) = 20–30%.

*Using 45-nm ZrO_x/indium-tin-oxide substrates.

[†]IGZO 1:0.11:0.29.

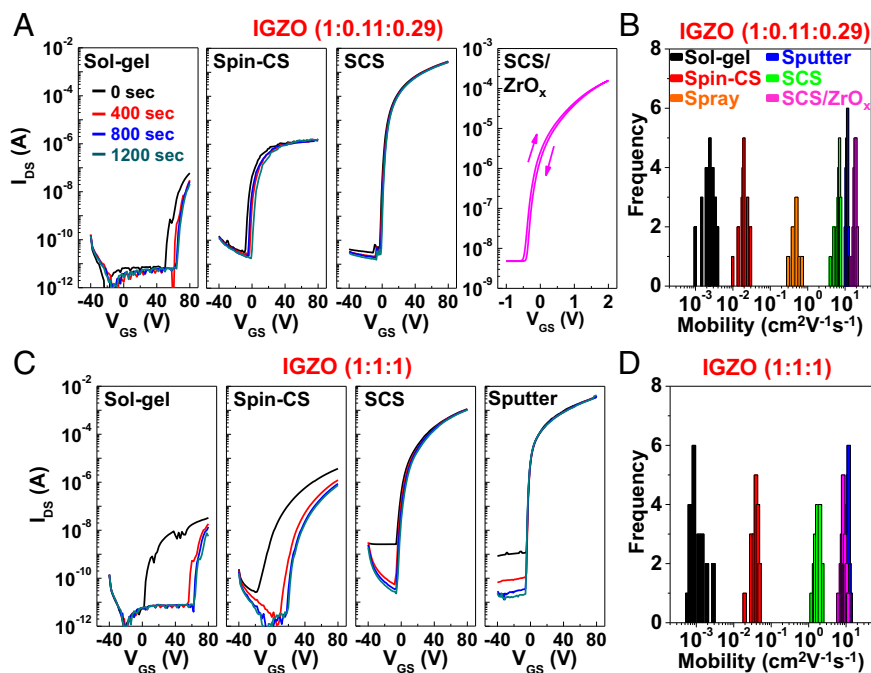


Fig. 3. Transfer characteristics ($V_D = 80$ V), bias stress data, and mobility distribution statistics for 50-nm-thick, single-layer IGZO TFTs fabricated by the indicated deposition methods. (A) IGZO composition (1:0.11:0.29) on Si/SiO_2 substrates (panel 4: SCS IGZO/ ZrO_x) annealed at 300 °C. (B) Corresponding mobility statistics (for sputter; 1:1:1 composition). (C) IGZO composition (1:1:1) on Si/SiO_2 substrates annealed at 350 °C. (D) Corresponding mobility statistics.

($\mu \sim 10^{-3}$ – 10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$), even after 350 °C annealing, whereas the SCS devices exhibit $\mu_{\text{max}} = 2.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, $I_{\text{on}}/I_{\text{off}} \sim 10^6$, $V_T \sim 16$ V, and subthreshold swing ~ 3 V/decade. For 1:1:1 SCS IGZO with a ZrO_2 gate dielectric, $\mu_{\text{max}} = 10.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ (SI Appendix, Fig. S19). To our knowledge, this report is the first instance of mobilities $> 10 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for 1:1:1 IGZO solution processed at such low temperatures. Finally and importantly, TFT bias stress stability under identical protocols was investigated (Fig. 3A and C), and independent of composition, the sol-gel and spin-CS devices exhibit marked threshold voltage instability ($\Delta V_T > +20$ to ~ 60 V), implying large densities of trap states (29), whereas the corresponding shifts for SCS (ΔV_T , 1:0.11:0.29 = +1.3 V; ΔV_T , 1:1:1 = +1.8 V) and fully optimized sputtered TFTs ($\Delta V_T = +0.7$ V) are small and similar. The contact resistance for IGZO TFTs is typically very low, and the mobility channel length dependence is very weak (40). These results are impressive considering that patterning of the gate, the IGZO layer, or a passivation layer was not used. Next, photolithography-defined sputtered and SCS-processed devices were investigated, and not surprisingly, performance parameters, such as the off-currents (pA), $I_{\text{on}}/I_{\text{off}}$ ($\sim 10^9$ – 10^{10}), and ΔV_T (< 0.2 – 0.6 V at 60 °C), were even further enhanced (SI Appendix, Figs. S17 and S18).

IGZO Film Microstructure and TFT Response. To understand the basis of the impressive SCS TFT performance, XRR, XPS, PAS, and C-V

analyses were carried out. XRR analysis assays film electron density and yields the mass density (Fig. 4A and B and SI Appendix, Fig. S20) (41). For the 1:0.11:0.29 IGZO films, the density monotonically increases with $\rho_{\text{spin-CS}} (4.53 \text{ gcm}^{-3}) < \rho_{\text{sol-gel}} (5.09 \text{ gcm}^{-3}) < \rho_{\text{SCS}} (6.13 \text{ gcm}^{-3})$, confirming that SCS achieves greater densification for the same 300 °C processing temperature. For 1:1:1 IGZO films, the order again is $\rho_{\text{spin-CS}} (3.57 \text{ gcm}^{-3}) < \rho_{\text{sol-gel}} (3.78 \text{ gcm}^{-3}) < \rho_{\text{SCS}} (5.20 \text{ gcm}^{-3}) < \rho_{\text{sputtering}} (5.66 \text{ gcm}^{-3})$ for tracking TFT performance. Obviously, the lower 1:1:1 vs. 1:0.11:0.29 density primarily reflects the lower high-Z indium content. XPS further supports these trends (SI Appendix, Fig. S21), indicating the greater densification of the SCS films vs. the spin-CS/sol-gel films. For the SCS-derived 1:1:1 and 1:0.11:0.29 IGZO samples, the M-O-M lattice content (41% and 56%, respectively) is greater than that of both the spin-CS and sol gel ($\sim 30\%$ and $\sim 50\%$, respectively). Furthermore, the SCS M-O-M content of the 1:0.11:0.29 IGZO composition (56%) approaches that of the sputtered 1:1:1 films (58%). These results indicate that more In-rich IGZO compositions have increased M-O-M content in these solution-processed films. Thus, the role of In in enhancing TFT transport is by not only forming more O vacancies (42) but also, reducing porosity and structural defects, as supported quantitatively by the PAS data (vide infra). This result plausibly reflects, among other factors, the lower lattice formation enthalpy (43) of In_2O_3 vs. Ga_2O_3 by almost 1,700 kJ mol^{-1} , enabling In-rich

Table 2. Performance metrics of 50-nm single-layer IGZO TFTs on 300-nm SiO_2/Si substrates with Al source/drain electrodes fabricated by the indicated methods at 300 °C (IGZO 1:0.11:0.29) and 350 °C (IGZO 1:1:1)

Deposition method	IGZO 1:0.11:0.29					IGZO 1:1:1				
	Mobility (cm^2/Vs)	V_T (V)	V_{ON} (V)	$I_{\text{on}}/I_{\text{off}}$		Mobility (cm^2/Vs)	V_T (V)	V_{ON} (V)	$I_{\text{on}}/I_{\text{off}}$	
Sol gel	$2.3 \times 10^{-3} \pm 3.0 \times 10^{-4}$	58.7 ± 9.6	51.6 ± 9.9	$\sim 10^3$ – 10^4		$1.1 \times 10^{-3} \pm 2.3 \times 10^{-4}$	47.1 ± 11.4	31.1 ± 10.9	$\sim 10^3$ – 10^4	
Spin-SC	$1.9 \times 10^{-2} \pm 2.1 \times 10^{-3}$	31.9 ± 9.5	23.7 ± 9.8	$\sim 10^4$ – 10^5		$3.7 \times 10^{-2} \pm 2.4 \times 10^{-3}$	35.5 ± 8.1	2.4 ± 8.9	$\sim 10^4$ – 10^5	
Spray	0.53 ± 0.2	7.6 ± 6.5	-3.3 ± 6.3	$\sim 10^3$ – 10^4		—	—	—	—	
Sputter	—	—	—	—		10.9 ± 0.12	2.2 ± 1.9	-5.8 ± 1.7	$\sim 10^6$ – 10^8	
SCS	6.8 ± 0.97	5.7 ± 2.8	-4.1 ± 2.5	$\sim 10^6$ – 10^7		1.8 ± 0.24	15.6 ± 4.0	-5.3 ± 3.7	$\sim 10^6$ – 10^7	
SCS*	19.1 ± 1.58	0.05 ± 0.04	-0.49 ± 0.04	$\sim 10^3$ – 10^5		8.4 ± 0.99	0.54 ± 0.08	-0.17 ± 0.07	$\sim 10^3$ – 10^4	

Average of ≥ 20 devices (except for spray: 10 devices). Measured in ambient conditions: RH = 20–30%.

*Using 45-nm $\text{ZrO}_x/\text{indium-tin-oxide}$ substrates.

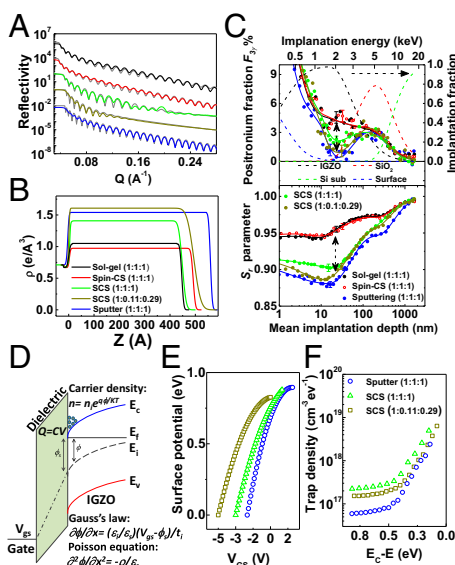


Fig. 4. Microstructural characterization of IGZO films. (A) XRR plots and (B) corresponding electron densities profiles of the indicated IGZO films. (C) PAS S_r and $F_{3\gamma}$ parameters for IGZO films deposited on SiO_2 (300 nm)/Si as a function of the positron mean implantation depth (implantation fraction for each layer of IGZO). (D) Representation of the energy band bending as a function of gate voltage in IGZO films. (E) Surface potential vs. gate voltage and (F) trap density states as a function of $E_c - E$ for the indicated IGZO compositions.

compositions to more readily reorganize and densify during low-temperature solution-phase MO precursor decomposition.

PAS was next applied to quantify the IGZO film porosity. This technique is sensitive to voids and can detect isolated and buried pores as small as 0.3 nm (44, 45). In amorphous porous IGZO films, the implanted positrons interact with electrons to form positronium (Ps) atoms that enable nanometer-scale porosity mapping over the entire film thickness. Fig. 4C shows results for the fraction of three- γ ortho-Ps annihilations ($F_{3\gamma}$) and the shape or S_r parameter as a function of mean positron implantation depth for SCS 1:1:1 and 1:0.11:0.29 IGZO films. Also shown are the positron implantation fraction distributions in each layer: surface, IGZO, SiO_2 , and Si substrate for the 1:1:1 SCS samples. Almost 95% of the 1- to 2-keV positrons are implanted in the film (SI Appendix). $F_{3\gamma}$ evolution between ~ 10 to ~ 50 nm, encompassing the IGZO film and the IGZO/ SiO_2 interface, identifies large Ps fractions for the 1:1:1 sol-gel and spin-CS films, where the process is far less efficient ($F_{3\gamma} \rightarrow 0$), 1:1:1 sputtered and 1:0.11:0.29 SCS films, and an intermediate case for 1:1:1 SCS films. Three- γ annihilations in the sol-gel and spin-CS samples indicate that ortho-Ps occupies empty cavities large enough to maintain the pick-off annihilation rate λ_{po} at a level not significantly larger than the self-annihilation rate $\lambda_{3\gamma}$ (46). The lower limit of cavity diameter to observe three- γ annihilation is ~ 1 nm (46, 47). This effect is observed in the amorphous SiO_2 of all samples (bump centered at ~ 170 nm in Fig. 4C).

Generally, the PAS S_r parameter depends on the annihilation site chemical environment and defect concentrations (vacancies, voids, and pores). The direct correlation between this parameter and the ortho-Ps fraction $F_{3\gamma}$ in Fig. 4C clearly indicates that, in these amorphous films, S_r values depend mainly on porosity. Thus, higher S_r values in the IGZO films correspond to higher Ps formation (para-Ps and ortho-Ps pick-off that annihilates in two γ -rays) (48). Quantitative evaluation is provided by fitting the data S_r evolutions in Fig. 4C (SI Appendix). From the XRR-derived IGZO film thicknesses, the film PAS mass densities are estimated by minimizing the variance of the model fits (χ^2_R plots in SI Appendix, Fig. S22B), yielding densities in good quantitative agreement with the XRR results (SI Appendix). The $F_{3\gamma}$ and S_r results confirm that the 1:0.11:0.29 SCS and 1:1:1 sputtered IGZO films are the least porous

(49), with the subnanometer porosities of the 1:0.11:0.29 SCS and 1:1:1 sputtered films estimated as $\sim 6\%$ with a mean pore size (Φ) of ~ 0.4 – 0.6 nm and a cavity number density (η) of $\sim 9 \times 10^{20} \text{ cm}^{-3}$ followed by a 1:1:1 SCS porosity of $\sim 10\%$ ($\Phi = 1$ – 2 nm; $\eta = \sim 2 \times 10^{20} \text{ cm}^{-3}$). The sol-gel and spin-CS film porosities are $>15\%$, with $\Phi = 2$ – 3 nm and $\eta = \sim 1 \times 10^{20} \text{ cm}^{-3}$ (SI Appendix). These results underscore the great importance of porosity, along with composition, for optimizing solution-processed IGZO film properties.

To complement the film microstructure data, C-V measurements (SI Appendix, Fig. S23) were performed to estimate trapped carrier densities and their energy profiles (Fig. 4D), allowing a density of states (DOS) distribution estimate near the conduction band edge (E_c) (50, 51). From the C-V data, the semiconductor insulator surface potential, ϕ_s , and surface potential gradient, $(d\phi/dx)_s$, are calculated for each gate voltage (Fig. 4E and F), providing boundary conditions to solve Poisson's equation and determine the potential distribution within the films (SI Appendix). Because of the low mobilities of the 50-nm sol-gel and spin-CS IGZO films, their capacitance modulation by the gate voltage is slow and unstable, indicating very high trap densities, corroborated by the large threshold voltage and V_T shifts in bias measurements. Accurate DOS extraction is, therefore, impossible, and we focus on comparing SCS and sputtered IGZO films (Fig. 4F), which are characterized by an exponential tail of states close to E_c and an approximately constant density for deeper level states in agreement with the literature (50). The sputtered IGZO films exhibit a DOS = $6.0 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$ away from E_c (deep traps), whereas both 1:1:1 and 1:0.11:0.29 SCS IGZO films have slightly greater deep trap densities of $\sim 2.2 \times 10^{17}$ and $1.5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$, respectively. High densities of deep traps can lower TFT off-state currents and also, reduce the subthreshold slope, which is suggested in the corresponding transfer plots (SI Appendix, Fig. S23). On the side near E_c , shallow trap states (tail states) dominate oxide TFT mobilities and bias stress stability. Here, the sputtered IGZO shows the lowest density of tail states ($\sim 2.0 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ at 0.15 eV below E_c), comparable to published pulsed laser-deposited (52) and sputtered film data (50, 53, 54). The best SCS devices (1:0.11:0.29 IGZO) exhibit shallow trap state densities similar to sputtered IGZO ($\sim 2.4 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ at 0.15 eV below E_c). The low 1:0.11:0.29 SCS IGZO tail state density is consistent with the large mobilities in Table 2 and the good bias stress stability in Fig. 3. Note that, for the 1:1:1 SCS IGZO system, the shallow trap density at 0.15 eV below E_c is $\sim 5.1 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$, more than two times that of 1:0.11:0.29 SCS IGZO, accounting for the lower TFT performance. Thus, these XRR, XPS, PAS, and C-V data connect the electronic structure aspects of IGZO films to composition and the aforementioned microstructural features and indicate that SCS is, to date, the only known solution process method capable of fabricating MO films with a process flow and TFT quality rivaling that of sputtered films.

Conclusions

An efficient low-temperature oxide film growth methodology combining combustion synthesis and spray coating is reported. SCS enables scalable fabrication of technologically relevant oxide films and film requisite thicknesses in a single deposition step within minutes. High-quality, nanoscopically dense, macroscopically continuous films are produced for both crystalline and amorphous MO semiconductors and conductors, yielding high-performance TFTs for the former and high thin-film conductivities for the latter. Most important, using a rudimentary spray-coating device, SCS produces IGZO films and TFTs approaching those fabricated by optimized magnetron-sputtering protocols in performance. We believe that these results show the potential of SCS for implementation in FAB microelectronics and areas where nanoscopic MO films are required.

Methods

Precursor Solutions for SCS and Spin-CS. All reagents were used as received from Sigma-Aldrich. These solutions were prepared with $\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$, $\text{Zn}(\text{NO}_3)_2 \cdot x\text{H}_2\text{O}$, and $\text{Ga}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$ in 2-methoxyethanol to yield 0.05 or 0.5 M

solutions. For 0.05 (or 0.5) M solutions, 55 (or 110) μL NH_4OH and 100 (or 200) μL acetylactone were added to 10 (or 2) mL precursor solutions and stirred overnight at 25 $^{\circ}\text{C}$. Before spin or spray coating, the precursor solutions were combined in the desired molar ratios and stirred for 2 h. All depositions were carried out at RH < 30%.

SCS. Substrates were maintained at 200–350 $^{\circ}\text{C}$ on a hot plate, whereas 0.05 M precursor solutions were loaded into the spray gun and sprayed intermittently (60-s cycles) on the substrates until the desired thickness (20 or 50 nm) was obtained. The drop sizes were between 30 and 150 μm depending on the processing temperature. The nozzle–substrate distance was 10–30 cm. Details of MO film and device fabrication/characterization, instrumentation, and XRR, PAS, and DOS modeling are reported in [S1 Appendix](#). TFT characterization was performed under ambient conditions using an Agilent 1500 Semiconductor Parameter Analyzer. The mobility- μ was

evaluated in the saturation region from $I_{\text{DS}} = (WC_i/2L)\mu(V_{\text{GS}} - V_{\text{T}})^2$, where C_i is the insulator capacitance/unit area, V_{T} is the threshold voltage, and V_{GS} is the gate voltage. W and L are channel width and length, respectively.

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