

Printable Organic-Inorganic Nanoscale Multilayer Gate Dielectrics for Thin-Film Transistors Enabled by a Polymeric Organic Interlayer

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Here, a new approach to the layer-by-layer solution-processed fabrication of organic/inorganic hybrid self-assembled nanodielectrics (SANDs) is reported and it is demonstrated that these ultrathin gate dielectric films can be printed. The organic SAND component, named P-PAE, consists of polarizable π -electron phosphonic acid-based units bound to a polymeric backbone. Thus, the new polymeric SAND (PSAND) can be fabricated either by spin-coating or blade-coating in air, by alternating P-PAE, a capping reagent layer, and an ultrathin ZrO_x layer. The new PSANDs thickness vary from 6 to 15 nm depending on the number of organic-ZrO_x bilayers, exhibit tunable film thickness, well-defined nanostructures, large electrical capacitance (up to 558 nF cm⁻²), and good insulating properties (leakage current densities as low as 10⁻⁶ A cm⁻²). Organic thin-film transistors that are fabricated with representative p-/n-type organic molecular/polymeric semiconducting materials, function well at low voltages (<3.0 V). Furthermore, flexible TFTs fabricated with PSAND exhibit excellent mechanical flexibility and good stress stability, offering a promising route to low operating voltage flexible electronics. Finally, printable PSANDs are also demonstrated and afford TFTs with electrical properties comparable to those achieved with the spin-coated PSAND-based devices.

1. Introduction

Thin-film transistors (TFTs) are traditional components of active matrix display backplanes and are envisioned for producing other types of circuitry for sensor and RFID applications.^[1-5] A typical TFT consists of a gate electrode, a dielectric layer, a channel layer (n- or p-type semiconductor) and source/drain electrodes, where the most critical materials are the dielectric and the semiconductor since charge transport occurs in the channel layer in close proximity to the semiconductor-dielectric interface.^[1] The past two decades have witnessed significant progress in developing solution-processable organic/inorganic semiconductor-based TFTs driven by the possibility of high throughput printing them at low costs, at low temperatures, and having compatibility with mechanically flexible substrates.^[6-11] Nevertheless, despite the remarkable advances achieved, the major limitation of most printed TFTs is the high driving voltages required to reach useful drain currents (I_{DS} , see

Equation (1)) due to the relatively low semiconductor carrier mobilities and dielectric gate capacitance values available.^[7,12-14] Here W/L is the channel width/length, C_i is the dielectric capacitance per unit area, μ is the carrier

$$I_{DS} = \frac{W}{2L} \mu C_i (V_{GS} - V_{TH})^2 \quad (1)$$

mobility, V_{GS} is the source-gate voltage, and V_{TH} is the threshold voltage. Importantly, it is essential to achieve high TFT I_{DS} at low operating voltages for real-world applications in flat panel displays, RF-ID tags, and portable electronics.^[15,16] Without changing device geometry (W and L) and the semiconductor material (μ), the most straightforward approach to overcome mobility/driving voltage limitations is to increase the capacitance C_i of the gate dielectric, by either increasing the dielectric constant (k) of the material or decreasing the thickness (d) of the gate dielectric layer (see Equation (2)).^[17,18]

$$C_i = \epsilon_0 \frac{k}{d} \quad (2)$$

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Among the several promising high- k materials reported in the literature, most using metal oxides,^[7,19–21] this laboratory invented a family of robust, structurally well-defined self-assembled nanodielectrics (SANDs), which not only have relatively high dielectric constants ($\kappa_{\text{org.}} \approx 7$) and high-breakdown thresholds ($E_{\text{BD}} \approx 6 \text{ MV cm}^{-1}$), but also thicknesses below 20 nm, thus affording high capacitance values combined with facile fabrication by solution-processing, and broad compatibility with diverse semiconductor families.^[12,22–27] The most advanced SAND consists of four alternating organic ($\approx 1.5 \text{ nm}$)-metal oxide ($\approx 2.5 \text{ nm}$) bilayers fabricated at a maximum temperature range of ≈ 150 – $220 \text{ }^{\circ}\text{C}$ on an electrical contact functioning as the gate electrode coated with a $\approx 3 \text{ nm}$ metal oxide primer layer. SAND-based TFTs exhibit high performance and function at low driving voltages.^[24] However, the organic layer is self-assembled by immersing the substrate in the organic component solution for $\approx 1 \text{ h}$, and the metal oxide nanolayer is then deposited by spin-coating (see representative fabrication details in ref. [12]), which limits the simplicity and processing efficiency, especially for large area applications.^[12] Furthermore, SAND-based TFT mechanical stress characteristics are unknown.

Inspired by the development of printable polymeric semiconductors and dielectrics, offering distinct advantages compared to their molecular counterparts,^[4,8,28,29] intriguing questions concern whether and how a SAND precursor might be rendered polymeric, whether the coating process can be simplified, and whether the resulting devices preserve excellent SAND dielectric and charge transport performance. In this contribution, we demonstrate a new approach to realize fully spin-coatable/printable polymer-based SANDs (PSANDs) as gate dielectrics for TFTs using phosphonic acid-functionalized organic polymeric precursors combined with nanoscale layers of high- k zirconium oxide (ZrOx). Both reagents are well-suited for ambient atmosphere fabrication of SAND multilayers, and the resulting P-SANDs exhibit high capacitance values up to 558 nF cm^{-2} and low leakage current densities ($\approx 10^{-6}$ – $10^{-7} \text{ A cm}^{-2}$ at 2 MV cm^{-1}). PSAND-based organic transistors exhibit good performance with both p-/n-type and small molecule/polymer semiconductors. More importantly, PSAND TFTs fabricated on polyimide (PI) substrates exhibit excellent mechanical flexibility, providing a new methodology for printable high-capacitance flexible dielectrics for unconventional electronics. Finally, large area uniform coating and well-defined layer formation using PSANDs are also accessible via a printing compatible process. Thus, blade-coating is successfully used here to fabricate entire PSAND TFT stacks exhibiting microstructure and device performance comparable to that fabricated by spin-coating.

2. Results and Discussion

In this section we first report the design rationale and realization of PSAND films fabricated by spin-coating. These newly developed dielectric films are next systematically characterized by optical (UV-vis), electrical [leakage current density vs voltage (I – V), capacitance versus voltage (C – V), and capacitance versus frequency (C – F) characteristics], and morphological (AFM) measurements. To demonstrate broad applicability to organic

thin-film transistor (OTFT) applications, p-/n-channel OTFTs based on both small molecules and polymeric organic semiconductors are fabricated and the device performance parameters are discussed in detail. Next, to demonstrate mechanical flexibility, we report PSANDs/OTFTs fabricated on flexible polyimide substrates and assess performance stability in bendability tests. Finally, we demonstrate printed PSANDs and their integration into printed OTFTs.

2.1. PSAND Film Deposition and Characterization

In order to realize fully spin-coated/printed SANDs, we first designed and attempted the synthesis of the polymeric organic precursor of PSAND, (P-PAE, see structure in **Figure 1**) which would simultaneously have, in addition to a polymeric backbone, the polarizable π -electron “push-pull” electronic structure of conventional SAND precursors provided by a quaternized stilbazolium salt as well as the capability to self-assemble on a metal oxide surface via the phosphonic acid group. Unfortunately, we were unable to characterize/utilize this new polymer (Figure 1) since it is completely insoluble in all common organic solvents, thus it could not be solution-processed. As a consequence, a new approach was developed which involves the use of linker reagent 4 and the stilbazole polymer P-PA to achieve, in a two-step spin-coating sequence, the *in situ* formation of P-PAE (vide infra, **Figure 2**). Briefly, the phosphonic acid-based π -electron building block 2 was synthesized as described in our previous study (**Scheme 1**)^[12] and next converted into the linker 3 as described in Section 4. The new polymer P-PA, formally the precursor of P-PAE, was synthesized starting from 2-(methylphenylamino)ethanol followed by functionalization with a methacryloyl chloride end group, essential for polymerization. The resulting amine 5 is then employed in diazo coupling with an aminopyridine reagent in acceptable yields, affording compound 6. Finally, the P-PA was synthesized by free radical polymerization of 6 by addition of azobisisobutyronitrile. All new compounds were characterized by conventional analytical techniques (^1H NMR, ^{13}C NMR, ^{31}P NMR, HRMS, and elemental analysis).

Before organic thin film deposition experiments, the thermal stability of the P-PA polymer and the linker were examined by the thermogravimetric analysis (TGA). As shown in the Figure S1, Supporting Information, P-PA has a decomposition temperature (T_d) of $262 \text{ }^{\circ}\text{C}$, and that of the linker is $267 \text{ }^{\circ}\text{C}$. These temperatures are far above those used for PSAND film processing. Next, PSANDs with n (organic-MO) bilayers ($n = 1$ – 4) were fabricated utilizing Linker + P-PA and ZrOx as the organic and metal oxide layer, respectively, and the fabrication procedure (for spin-coating) is shown in Figure 2. Organic-MO bilayer fabrication first requires the deposition of a ZrO_x primer layer on a the substrate of choice (Si⁺⁺, glass, or Au-PI), which is spin-coated on the substrate using a ZrCl₄ precursor solution (0.02 M, ethanol) in a humidity-controlled glove box filled with air (RH $\approx 20\%$). Next, the linker monolayer is spin-coated on the ZrO_x primer layer from a 4 mg mL^{-1} chloroform solution, annealed at $110 \text{ }^{\circ}\text{C}$ for 20 min, followed by rinsing with dichloromethane twice to remove an excess amounts of the linker. Then, P-PA is spin-coated (4 mg mL^{-1} in chloroform)

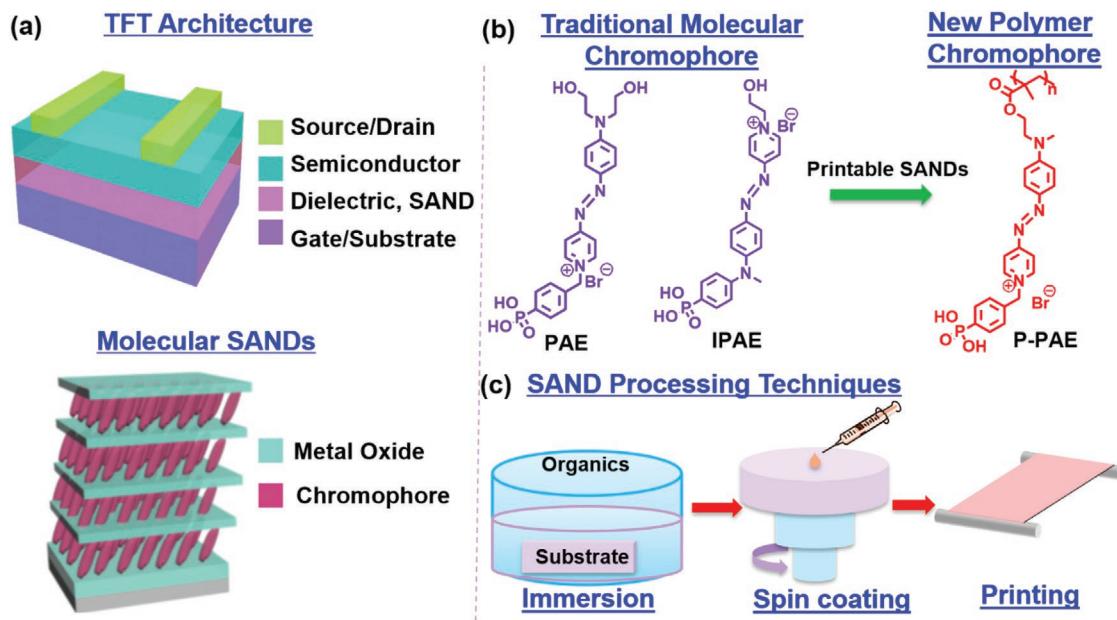


Figure 1. TFT and SAND architectures, organic compounds for SANDs, and their processing techniques.

and subjected to a thermal annealing at 110 °C for 20 min to achieve the N-quaternization reaction on the surface, again, followed by rinsing with dichloromethane twice to remove unreacted P-PA. Finally, the ZrO_x interlayer is deposited by the same method as the primer layer yielding the PSAND-1. PSAND-2, -3, and -4 nanostructures by alternating repetition of the linker, polymer, and ZrO_x layer depositions.

The effectiveness of the present iterative process (Figure 2) and the resulting multilayer (PSAND-1 \approx 4) structural regularity was verified by a full complement of physicochemical techniques, including: 1) UV-visible spectroscopy (UV-vis) to characterize the assembly chemistry and microstructural regularity; 2) X-ray reflectivity (XRR) to measure the film thickness, interface quality, and film density; 3) AFM to examine surface morphology and roughness. The absorption spectra of PSAND- n were measured for samples grown on glass

substrates (Figure 2). The optical absorption spectrum of a P-PA film on glass (Figure 3a) exhibits a maximum absorption peak (λ_{max}) centered at 430 nm. Upon reaction of P-PA with the coupling reagent on the PSAND- n surface, the λ_{max} red-shifts to \approx 450 nm. Although a bathochromic shift is expected upon N-quaternization, this value is at far higher energy than that of typical stilbazolium salt chromophores and traditional SAND-1 ($\lambda_{max} \approx$ 560 nm, Figure S2, Supporting Information).^[24] This result is reasonable since it is unlikely that all PA units in P-PA are quaternized as in conventional SAND synthesis where the reaction is driven by molecular self-assembly, and therefore only quaternized chromophores remain on the surface. Thus, we first attempted to quantify the degree of quaternization using XPS, however, the result is inconclusive (Figure S2, Supporting Information). Therefore, we deconvoluted the optical spectra of PSAND- n in Figure 3a using those of the (neutral)

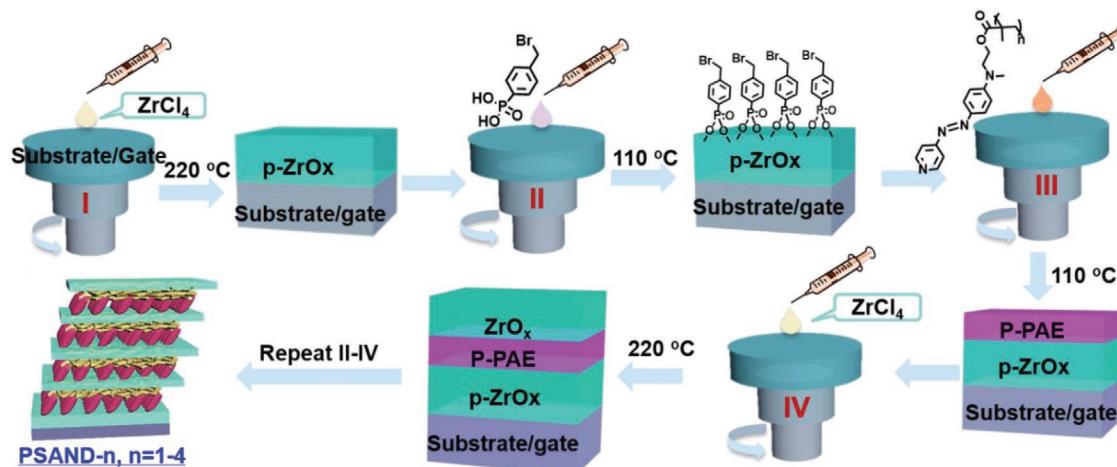
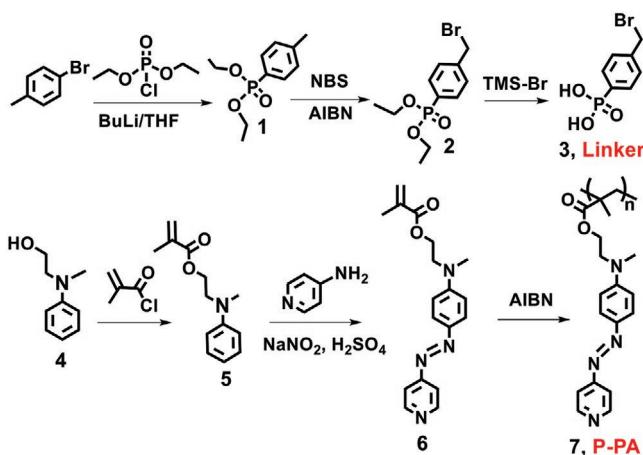


Figure 2. The PSAND gate dielectric solution growth process employed in this study.



Scheme 1. Synthesis of the Linker reagent and the polarizable stilbazole phosphonic acid polymer P-PA.

P-PA and (quaternized) PAE compounds (Figure S2c, Supporting Information). Details of the analysis are reported in the

Supporting Information. The data indicate that only \approx 12–13% of the N atom are quaternized, a result corroborated also by a combined ^1H NMR/optical analysis of a partially alkylated P-PA polymer (see Figure S2d, Supporting Information, for details). These data also indicate that the P-PA reacts with the linker group, and a polymeric chromophore grows on the surface of ZrO_x . Furthermore, despite the low quaternization density, the attachment density is amply sufficient to anchor the polymer chains to the surface and form a robust organic layer on top of the oxide. Importantly, the absorbance intensity at \approx 450 nm increases linearly with increasing numbers of PSAND bilayers (Figure 3a inset), thus that essentially an equal density of chromophore units are incorporated within each organic sub-layer of PSAND up to the fourth P-PAE + ZrO_x bilayer. This result is identical to our previous study on small molecule-based SANDs,^[12] implying that a fully spin-coatable SAND can be realized by employing this new strategy.

Encouraged by the findings from the UV-vis characterization, XRR measurements on PSANDs on Si^{++} were next carried out. The XRR data and fitting analysis are shown in Figure 3b as a function of the out-of-plane scattering vector $q = 4\pi \sin \theta / \lambda$,

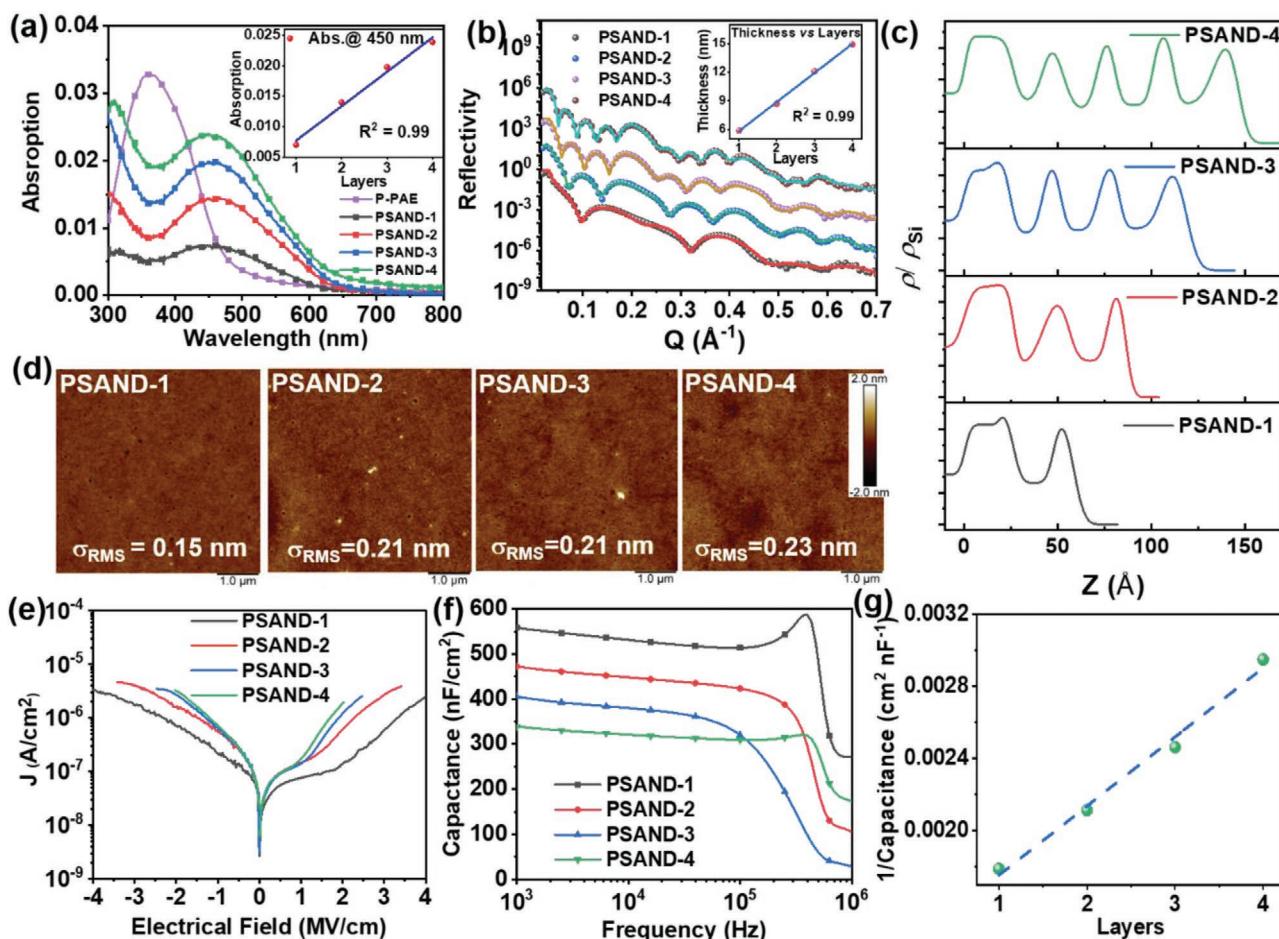


Figure 3. a) UV-vis absorption spectra of PSAND- n ($n = 1, 2, 3, 4$) on glass; the insert is the absorption peak (450 nm) intensity of PSAND- n as a function of the number of bilayers. b) X-ray reflectivity curves and theoretical fittings, along with c) electron density profiles for PSANDs. d) AFM height images of PSANDs. e) Leakage current density versus electric field (J vs E) for PSANDs. f) Capacitance versus frequency (C - F) curves (measured at bias voltage of 3 V). g) Reciprocal of capacitance versus the number of PSAND layers with the corresponding linear fit indicated by the dashed line.

with least-squares best-fit models calculated with the Abeles matrix method using the Motofit software package.^[30,31] The corresponding fits are shown overlaid on the corresponding experimental data, demonstrating a clear difference when the number of bilayer increases, where the thicker PSANDs show greater reflectivity oscillations. In Figure 3c, the extracted electron density profiles reveal highly ordered multilayers, which are consistent from sample to sample in terms of electron density, roughness, and thickness. All of the ZrO_x and organic interfaces are at comparable positions along the out-of-plane direction, indicating highly controlled, sequential deposition which is similar to previous reports using molecular organic precursors.^[12] The PSAND-1, 2, 3, and 4 film thickness are found to be 5.9, 8.7, 12.1, 14.9 nm, respectively, as derived from the individual electron density profiles. The thickness of the ZrO_x primer layer is ≈ 2.5 nm while that of the ZrO_x capping interlayer is ≈ 1.1 nm for all samples, values consistent with the MO precursor concentrations (0.02 vs 0.01 M). More importantly, the total thickness increases linearly with the layers of PSANDs, indicating highly uniform and reproducible thin films (Figure 3b inset).

The surface morphologies of PSAND-*n* samples were next imaged by AFM starting with those of the primer ZrO_x layer, ZrO_x + linker and ZrO_x + linker + polymer (Figure S3, Supporting Information). Both the primer ZrO_x and the ZrO_x + linker exhibit extremely smooth surfaces with root-mean-square roughnesses (σ_{RMS}) of ≈ 0.10 nm. After first P-PAE growth the film becomes slightly rougher with a $\sigma_{\text{RMS}} = 0.14$ nm. Interesting, when increasing the number of bilayers from 1 to 4, thus moving from PSAND-1 to PSAND-4, the film surface remains ultra-smooth with a σ_{RMS} remaining ≈ 0.20 nm, which is beneficial for the charge transport in a TFT architecture. Thus, all these characterizations indicate that these newly developed PSANDs are good candidates for dielectrics in TFTs.

2.1.1. PSAND-*n* Dielectric Properties

Next, metal–insulator–semiconductor (MIS) devices were fabricated by contacting n^{++} -Si/PSAND-*n* with Au electrodes (dimension: $200 \times 200 \mu\text{m}^2$; see Section 4 for details). First, the leakage current of the PSAND films was measured. Figure 3e shows the current density versus electric field (J – E) plots for PSAND-*n* (*n* = 1, 2, 3, 4), which indicate that for a given electric field (E) the leakage current density initially increases with *n* and then saturates at $\approx 10^{-6} \text{ A cm}^{-2}$ for $E = 2 \text{ MV cm}^{-1}$ (Figure 3e and Figure S4, Supporting Information). Similar to our previous SAND results, we find that PSAND-1 exhibits

the lowest leakage current density (PSAND-2-4), which can be ascribed to the synergistic effects of the additional leakage barriers from the Si native oxide and the ZrO_x primer layer.^[12] However, it will be seen experimentally that this effect attenuates for thicker PSANDs. Furthermore, the leakage current densities of the newly developed PSANDs are lower than that of bulk ZrO_x films grown by the same sol–gel method at moderate processing temperatures ($\approx 220^\circ\text{C}$) (Figure S4a, Supporting Information).^[32] The breakdown electric field was also measured (Figure S4, Supporting Information) and found to range from 10.52 MV cm^{-1} for PSAND-1, 8.39 MV cm^{-1} for PSAND-2, 9.01 MV cm^{-1} for PSAND-3, 8.57 MV cm^{-1} for PSAND-4 (Table 1, Figure 3), which are very respectable metrics. Note, these dielectric films are only ≈ 6 – 15 nm thick and have been fabricated in an ambient/cleanroom-free environment, thus fabrication in well controlled FAB conditions should further enhance dielectric strength.

Capacitance–frequency (C – F) measurements were next performed on the MIS structures, and the measured capacitances are 558 (PSAND-1), 472 (PSAND-2), 406 (PSAND-3), and 339 nF cm^{-2} (PSAND-4) at 10^3 Hz (Figure 3f, Figure S5, Supporting Information, and Table 1). Note that these values remain constant when varying the applied frequency from 10^3 to 10^5 Hz , which is important for an accurate mobility calculation in TFTs. The reciprocal value of C_i versus PSAND-*n* (*n* = 1, 2, 3, and 4) plot (Figure 3g) shows a linear increase with the number of bilayers, which supports the evolution of well-structured and regularly-defined multilayer architectures. Additionally, the dielectric constant of the polymeric organic layer, P-PAE in PSAND, was also calculated. The multilayer dielectric in the n^{++} -Si/ PSAND [primer ZrO_x /(P-PAE/interlayer ZrO_x)*n*, *n* (the number of bilayer) = 1–4]/Au MIS devices can be modeled as capacitors in series, thus according to Equation (3). Here, SiO_2 is the native oxide (1.5 nm) on the Si wafer, p-ZrO_x is the ZrO_x primer layer, c-ZrO_x is the ZrO_x capping layer, and P-PAE is the organic layer, and *n* is the number of bilayers (*n* = 1, 2, 3, and 4). According to our previous studies, the capacitance of the native oxide and ZrO_x primer layer on the Si^{++} bottom electrode are 2236 and 4425 nF cm^{-2} , respectively, assuming a 1.5 nm thick SiO_2 (*k* = 3.9) and 2 nm thick ZrO_x layer (*k* = 10).^[33] Thus, using the aforementioned C_i of P-SAND-4 yields a *k* of ≈ 6 for P-PAE which is slightly lower than that in our previous studies (7–9).^[24] This result is consistent with the lower degree of N-quaternization, which reduces the overall molecular polarizability of the organic layer.

$$\frac{1}{C_i} = \left(\frac{1}{C_{\text{SiO}_2}} + \frac{1}{C_{\text{p-ZrO}_x}} \right) + n \times \left(\frac{1}{C_{\text{P-PAE}}} + \frac{1}{C_{\text{c-ZrO}_x}} \right) \quad (3)$$

Table 1. Summary of film and dielectric properties for PSAND-1-4 films.

Dielectrics	Thickness [nm]	Roughness [nm]	J [$10^{-7} \text{ A cm}^{-2}$] at 2 MV cm^{-1}	C_i [nF cm^{-2}] at 10^3 Hz	C_i [nF cm^{-2}] at 10^3 Hz^a
PSAND-1	5.9	0.15	1.08	558	487
PSAND-2	8.7	0.21	4.72	472	432
PSAND-3	12.1	0.21	10.3	406	373
PSAND-4	14.9	0.23	17.4	339	327

^a)HMDS Capped.

Finally, note that for TFT fabrication (vide infra) all PSANDs were reacted with HMDS (see Section 4 for details) to passivate surface hydroxyl ($-\text{OH}$) groups as $-\text{OSi}(\text{Me})_3$ coatings before semiconductor deposition. This strategy affords a more hydrophobic and OH-free surface which typically reduces interfacial trap densities in OTFTs.^[34] As expected, the HMDS-capped PSANDs exhibit slightly lower C_i values [487 (PSAND-1), 432 (PSAND-2), 373 (PSAND-3), and 327 nF cm^{-2} (PSAND-4); $F = 10^3$ Hz] than those of the uncapped samples (see Table 1 and Figure S6, Supporting Information, for details) likely reflecting the slightly increased film thickness and reduction of the highly polarizable OH groups. Note that all OTFT mobilities were calculated using these C_i values.

2.2. Organic Thin-Film Transistors Using PSANDs

Encouraged by the aforementioned excellent dielectric properties of PSANDs, TFTs were fabricated with representative organic semiconductors, including pentacene (P5), copper(II) 1,2,3,4,8,9,10,11,15,16,17,18,22,23,-24,25-hexadecafluoro-29H,31H-phthalocyanine (F_{16}CuPc), N,N'-1H,1H-perfluorobutyl dicyanoperylenecarboxydiimide (PDIF-CN₂) and the polymer diketopyrrolopyrrole-dithienyl-thieno[3,2-b]thiophene (DPP-DTT, see structures in Figure 4a). These semiconductors were processed by vacuum vapor deposition, spin-coating, or blade-coating (see details in Section 4) on n⁺⁺-Si/ PSAND-*n* substrates. After semiconductor deposition Au source and drain contacts were deposited by thermal evaporation through a shadow mask to define the contact geometry ($L = 150 \mu\text{m}$ and $W = 1500 \mu\text{m}$). All TFT measurements were performed in ambient. Representative output and transfer I -V plots for our TFTs on PSAND-1-4 are shown in Figure 4b-e and Figures S7–S10, Supporting Information, while Table 2 summarizes the major electrical metrics. Typical transfer characteristics of the TFTs based on vapor-deposited P5 and F_{16}CuPc are shown in Figures 4c,d, respectively. Thus, PSAND-*n* P5 based OTFTs exhibit good performance with hole mobilities (μ_h s) of 0.36–0.40 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, threshold voltages (V_{TH}) in the range of -1.19 – -1.46 V, and on/off current ratios ($I_{\text{on}}/I_{\text{off}}$) of 10^3 – 10^4 . Also, the F_{16}CuPc TFTs exhibit very similar electron mobilities (μ_e s) of 0.019–0.023 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and V_{TH} of -1.14 – -1.34 V (Figure 4 and Figure S8, Supporting Information). The $I_{\text{on}}/I_{\text{off}}$ is only $\approx 10^1$, which is typical of unpatterned F_{16}CuPc OTFTs.^[24] Note also that PSANDs with different thicknesses exhibit minimal variations in OTFT performance, in agreement with the well-defined PSAND layer structure, stability, and similar interfacial chemistry. Also, these parameters are comparable to those in our previous studies on small molecule-based SANDs, which supports the utility of this new approach for fabricating high-quality nanodielectrics.^[24] Regarding solution-processed semiconductors, we selected DPP-DTT because of the amply established performance^[4,35,36] and PDIF-CN₂ considering the good transport and impressive air stability,^[37] which is important for the bottom gate, top contact device architecture employed in this study (Figure 4d,e; Figure S9 and S10, Supporting Information). Typical transfer plots for solution-processed DPP-DTT and PDIF-CN₂ TFTs on PSAND-*n* are shown in Figures 4d,e, respectively. Thus, the

p-channel DPP based TFTs with all PSANDs exhibit a very similar μ_h of 0.16–0.20 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, a similar V_{TH} of -1.30 – 1.84 V, and a good $I_{\text{on}}/I_{\text{off}}$ of 10^3 . For the n channel PDIF-CN₂TFTs, all devices show a very similar μ_e of 0.18–0.23 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ with a similar V_{TH} of -1.30 – 1.84 V, and $I_{\text{on}}/I_{\text{off}} \approx 10^2$.

Finally, the surface morphologies of all semiconductors were investigated by AFM to better understand the charge transport. As shown in the Figure 4, the vapor deposited P5 films exhibit very strong texturing with a σ_{RMS} of 7.65 nm, which is similar with that of other reports.^[12] In contrast, the vapor-deposited F_{16}CuPc films are far smoother with a σ_{RMS} of 1.28 nm, corroborating the reduced texturing and performance of this representative n-type semiconductor. Both solution-processed semiconductors exhibit very smooth morphologies with a σ_{rms} of 1.35 and 1.61 nm for DPP-DTT and PDIF-CN₂, respectively. However, the polymer films exhibit a typical fibrillar morphology while the PDIF-CN₂ films evidence formation of quite flat crystals. These results demonstrate that the newly developed PSANDs are good candidates as gate dielectrics for both vapor- and spin-coated OTFTs.

2.3. Flexible OTFTs Based on PSAND-4

To verify the mechanical flexibility of PSANDs, flexible capacitors as well as OTFTs based on the thickest PSAND (PSAND-4) films were fabricated on Au-coated polyimide (PI) substrates. The TFTs used DPP-DTT as the semiconductor and have the structure shown in Figure 5a (see processing details in the Section 4).^[26] The HMDS-capped PSAND-4 employed here was prepared using the same processing conditions as the ones fabricated on Si⁺⁺ substrates. The C_i of 327 nF cm^{-2} was used for the mobility calculation. Figure 5b shows typical transfer curves for the OTFT devices at various bending radii ($\infty \text{ mm} \rightarrow 1 \text{ mm}$). TFT metrics can be found in Tables S1 and S2 of the Supporting Information. The pristine DPP-DTT OTFTs fabricated on PI substrates exhibit good performance with a μ_h of 0.18 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, V_{TH} in the range of -0.21 V, and $I_{\text{on}}/I_{\text{off}}$ of 10^3 , values which are comparable to the rigid TFTs of this study. Upon progressively bending from ∞ to a 1 mm radius, the mobility remains stable at ≈ 0.2 V while the V_{TH} shifts from ≈ -0.3 to ≈ -0.7 V (Figure 5c). Importantly, these TFTs exhibit excellent mechanical flexibility with negligible performance loss after bending at 2 mm for 1000x (Figure 5d). This study demonstrates that the newly developed PSAND-4 exhibits excellent mechanical flexibility and is a good candidate for any other flexible electronics application requiring a more ductile dielectric material.

2.4. Printed PSAND Films and Devices

Finally, to demonstrate that SAND-like dielectric is printable, blade-coating (BC) was utilized for PSAND film growth as well as semiconductor layer deposition for TFT integration. The BC technique has advantages over spin-coating, including concurrent thermal annealing during film deposition, minimal precursor solution waste (reduced by $\approx 10\times$), and potential R2R scalability.^[27] To demonstrate the concept we fabricated

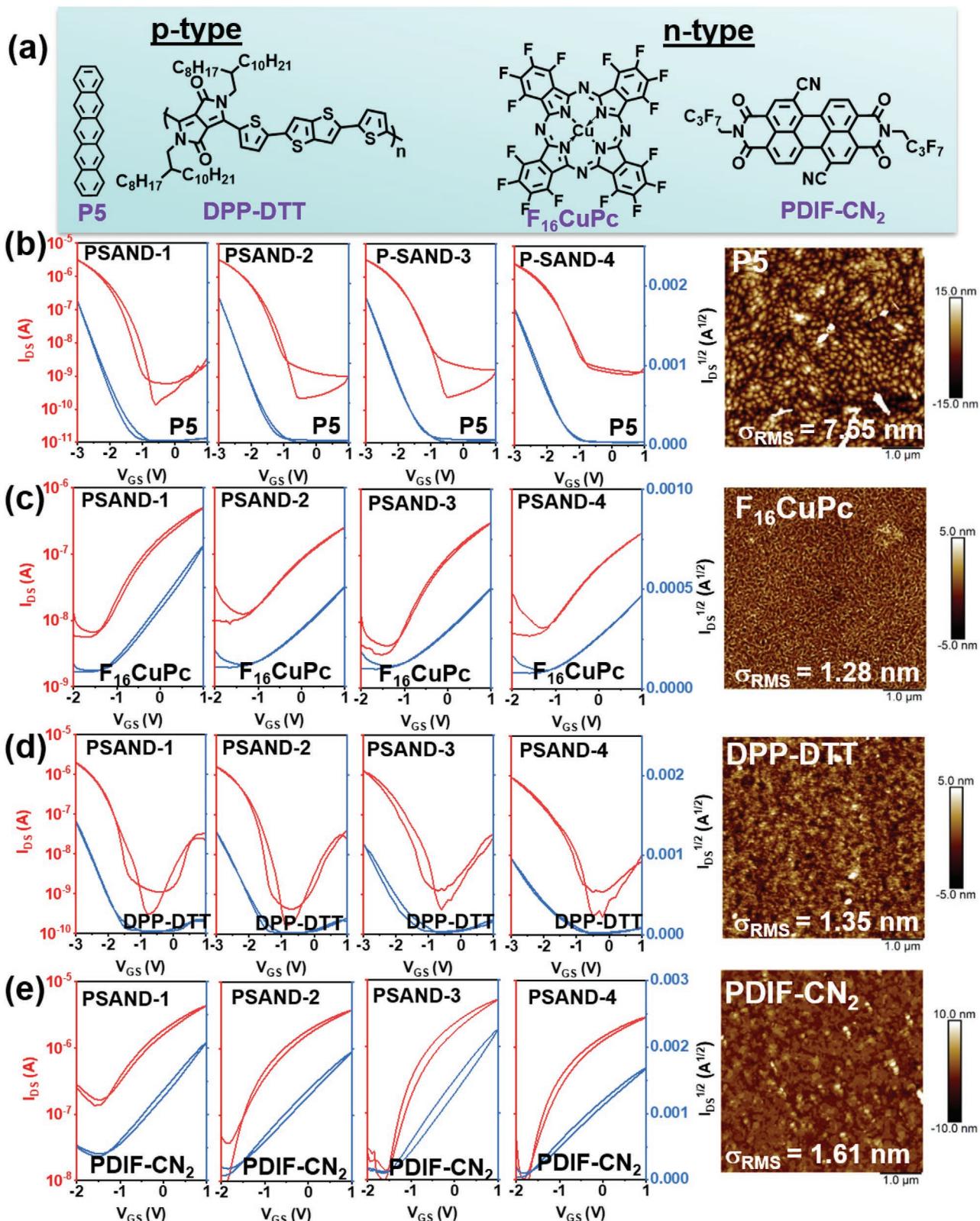


Figure 4. a) The chemical structures of organic semiconductors employed in this study, b–e) transfer characteristics of PSAND-x TFTs for the indicated semiconductors and the surface morphologies (height images by AFM).

Table 2. Performance parameters of OTFTs fabricated with the indicated PSANDs.

P5 (p-channel) ^{a)}				F ₁₆ CuPc (n-channel)				
PSAND-1	PSAND-2	PSAND-3	PSAND-4	PSAND-1	PSAND-2	PSAND-3	PSAND-4	
μ (cm ² V ⁻¹ s ⁻¹)	0.36 ± 0.02	0.37 ± 0.02	0.39 ± 0.02	0.40 ± 0.04	0.019 ± 0.002	0.023 ± 0.003	0.022 ± 0.002	0.020 ± 0.002
I_{ON}/I_{OFF}	10 ⁴	10 ⁴	10 ⁴	10 ³⁻⁴	10 ¹	10 ¹	10 ¹	10 ¹
V _{TH} (V)	-1.46 ± 0.03	-1.33 ± 0.03	-1.28 ± 0.05	-1.19 ± 0.04	-1.34 ± 0.26	-1.14 ± 0.07	-1.18 ± 0.29	-1.17 ± 0.27
V _{ON} (V)	-0.81 ± 0.10	-0.79 ± 0.10	-0.65 ± 0.12	-0.55 ± 0.15	-1.52 ± 0.23	-1.38 ± 0.37	-1.33 ± 0.28	-1.22 ± 0.23
DPP-DTT (p-channel)				PDIF-CN ₂ (n-channel)				
PSAND-1	PSAND-2	PSAND-3	PSAND-4	PSAND-1	PSAND-2	PSAND-3	PSAND-4	
μ (cm ² V ⁻¹ s ⁻¹)	0.20 ± 0.05	0.17 ± 0.04	0.16 ± 0.05	0.17 ± 0.03	0.23 ± 0.10	0.20 ± 0.03	0.25 ± 0.07	0.18 ± 0.012
I_{ON}/I_{OFF}	10 ³	10 ³	10 ³	10 ³	10 ¹	10 ²	10 ²	10 ²
V _{TH} [V]	-1.39 ± 0.26	-1.32 ± 0.20	-1.27 ± 0.09	-1.03 ± 0.12	-1.30 ± 0.78	-1.60 ± 0.29	-1.30 ± 0.37	-1.84 ± 0.03
V _{ON} [V]	-0.98 ± 0.10	-0.91 ± 0.20	-0.67 ± 0.20	-0.45 ± 0.12	-1.46 ± 0.22	-1.80 ± 0.18	-1.54 ± 0.13	-1.80 ± 0.14

^{a)}Average of ≥ 10 devices

PSAND-1 as a representative dielectric of this family. Thus, both primer and capping ZrO_x layers as well as the organic Linker and P-PA layers are deposited by BC using the procedures reported in Section 4. Briefly, the substrate (n⁺ Si) is placed on the blade-coater setup on a surface maintained at a temperature of 50–70 °C. The Zr precursor solution is then dispensed at the interface between the substrate and the blade until a meniscus forms. For the growth of premier ZrO_x (0.02 M, ethanol), the blade is horizontally transported at a constant velocity of 10 mm s⁻¹. Then the film is annealed at 220 °C for 20 min. For the deposition of the linker, the linker is dissolved in chloroform (4 mg mL⁻¹) and printed with a blade rate is 10 mm s⁻¹. After the substrates are annealed at 110 °C for 20 min, the

substrates are rinsed with dichloromethane twice. Finally, the P-PA is blade-coated on the linker surface at a blade rate of 10 mm s⁻¹ using a 4 mg mL⁻¹ chloroform solution followed by annealing at 110 °C for 20 min. Next, the substrate is rinsed with dichloromethane. Finally, the surface is capped with ZrO_x (0.01 M, ethanol) as described for the primer layer.

BC-PSAND-1 XRR data and fitting analysis are shown in Figure S11, Supporting Information, and the extracted electron density profiles reveal a highly ordered multilayer structure, which is similar with the results from the spin-coated PSAND-1. The total thickness of the BC PSAND-1 films is ≈6.1 nm, as derived from the individual electron density profiles. The surface morphologies of the different BC PSAND-1

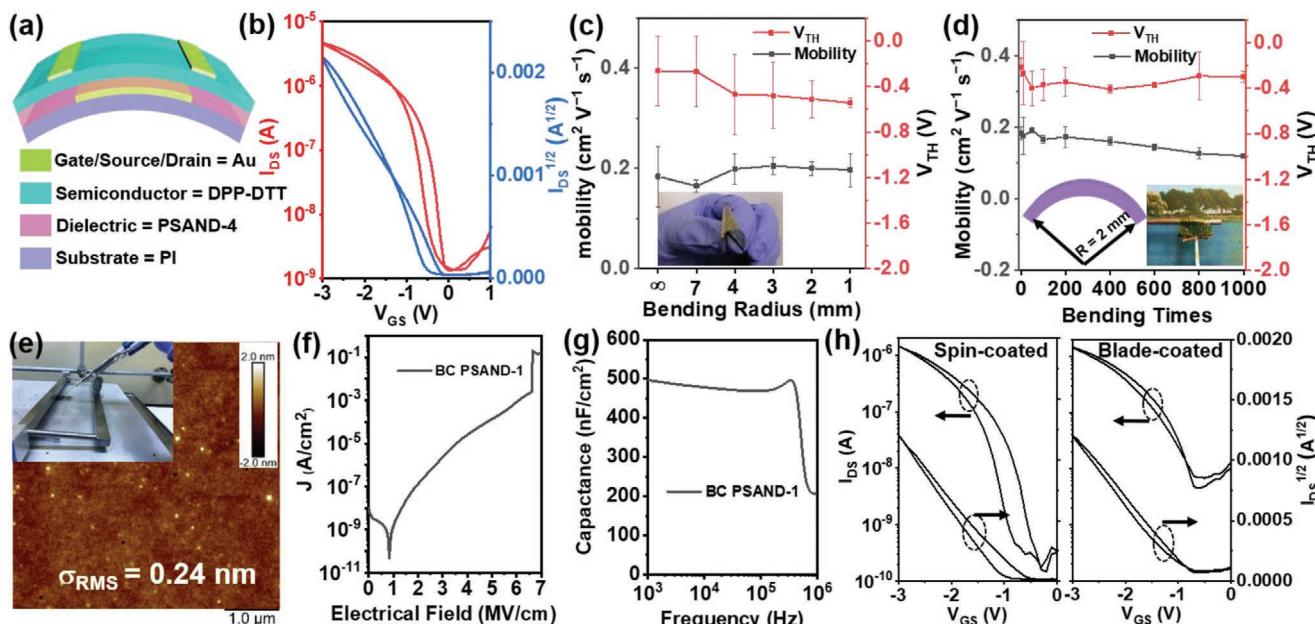


Figure 5. a) Device architecture used for flexible TFTs. b) Transfer curves and c) mobility variation of bottom-gate flexible TFTs on a PI substrate as a function of bending radius. (Inset) Photo of device under bending. d) Mobility and threshold voltage stability for bending test cycles with a radius of 2 mm. e) AFM height image for BC PSAND-1. (Inset) Photo of the BC process. f) Leakage current density versus electric field (J vs E) for PSANDs. g) Capacitance versus frequency (C-F) curves (measured at bias voltage of 3 V). h) Transfer curves for the BC TFTs.

layers were also investigated by AFM and indicated smooth surfaces, for example, a σ_{RMS} of 0.12 nm for BC prime ZrO_x layer (Figure S11, Supporting Information) and 0.24 nm for the completed BC PSAND-1 (Figure 5e), demonstrating that high-quality PSAND can also be realized by the BC technique. MIS electrical measurements indicate that the leakage current of the BC PSAND-1 dielectric is $\approx 10^{-6}$ A cm^{-2} at 2 MV cm^{-1} (Figure 5f). BC PSAND-1 exhibit strong tolerance to the applied electric field with a break-down field of ≈ 7 MV cm^{-1} . C-F measurements reveal that the C_i of the BC PSAND-1 is 497 nF cm^{-2} at 10^3 Hz (Figure 5g). Note, HMDS-capped BC-PSAND-1, used for TFT fabrication (see Section 4 for details) exhibits a C_i of 470 nF cm^{-2} (10^3 Hz, see details in Figure S11, Supporting Information). Finally, TFTs using the BC PSAND-1 as the gate dielectric and DPP-DTT as the semiconductor were fabricated by employing the device architecture depicted in the Figure 1. The semiconductor layer (DPP-DTT) is deposited both by spin-coating (control) and blade-coating (see Supporting Information for details). From the transfer curves in Figure 5h the performance of the spin-coated devices [$\mu_h = 0.11$ cm 2 V $^{-1}$ s $^{-1}$; $V_{\text{TH}} = -1.14$ V, $I_{\text{on}}/I_{\text{off}} = 10^4$] is comparable to the spin-coated PSAND-1 devices. Additionally, the all-BC processed OTFTs (Figure 5h) also exhibit respectable performance with a μ_h of 0.10 cm 2 V $^{-1}$ s $^{-1}$, thus approaching those of the conventional spin-coated platform.

3. Conclusions

Here we demonstrate the fabrication of ultra-thin PSANDs compatible with R2R fabrication methodologies. These layer-by-layer organic/inorganic PSANDs, independent of the synthesis method, exhibit similar thicknesses, surface morphologies, and dielectric properties. OTFTs were fabricated with various p-/n-type organic molecular/polymeric semiconducting materials using both spin-coating and blade-coating demonstrating good electrical characteristics. When fabricated on flexible substrates, good mechanical flexibility is also demonstrated. Thus, this work provides a new entry to the design and fabrication of ultra-thin gate dielectric films for flexible and printable electronics.

4. Experimental Section

Synthesis: The linker and the SAND polymer precursor P-PA were synthesized according to the synthetic route reported in Scheme 1. Synthetic details are reported in Supporting Information.

SAND Film Growth: ZrCl_4 solutions for the growth of ZrO_x layers (primer layer and capping layer) were prepared by dissolving 93.2 mg of ZrCl_4 in 4.0 mL of ethanol, affording a 0.1 M stock solution for further use. After 5 min of stirring, 100 μL of 68% wt./wt. HNO_3 was added and the solution was heated at 60 °C for 3 h, then stirred at room temperature for 12 h. Next, 0.01 and 0.02 M solutions were prepared by diluting the above stock solution with ethanol for future use. PSAND- n films were fabricated according to Figure 2 following the iterative deposition of the phosphonic acid-based linker layer and growth of the polymer layer, and the ZrO_x interlayer for capping and multifunction. Growth of PSAND- n films was carried out in the following steps: Step 1 (p- ZrO_x): The p- ZrO_x was prepared by spin-coating the 0.02 M precursor solution at 5000 rpm for 30 s on a given substrate (Si $^{++}$, glass or Au-PI)

in a humidity-controlled glove box under air ($\approx 20\%$), then the coated substrate was baked at 220 °C for 20 min. Step 2 (Linker monolayer deposition): The linker layer was grown by spin-coating linker precursor (4 mg mL $^{-1}$, CHCl_3) on the p- ZrO_x -coated substrate. The linker coated substrates were annealed at 110 °C for 20 min, followed by rinsing with CH_2Cl_2 twice to remove excess linker. Step 3 (P-PA deposition for N-quaternization): P-PA was spin-coated (4 mg mL $^{-1}$, CHCl_3) on the linker + p- ZrO_x substrates and subjected to a thermal annealing at 110 °C for 20 min to enable N-quaternization reaction, again, followed by rinsing with CH_2Cl_2 twice to remove unreacted P-PA. Step 4 (ZrO $_x$ -capping): The capping layer was fabricated by spin-coating the 0.01 M precursor solution at 5000 rpm for 30 s, then baked at 220 °C for 20 min. Steps 2–4 were repeated in sequence to achieve the desired number of PSAND- n layers.

HMDS Capping Layer Growth: The HMDS-capped PSAND films were fabricated by spin-coating (5000 rpm, 30 s) pure HMDS on top of PSAND- n ($n = 1, 2, 3$, and 4) films, followed by annealing at 130 °C for 20 min in ambient.

Metal-Insulator-Semiconductor Fabrication and Characterization: Gold contacts were thermally evaporated (40 nm, 0.1–0.2 Å s $^{-1}$, base pressure $6\text{--}7 \times 10^{-6}$ Torr) on the PSAND- n coated Si substrates through a 200 $\mu\text{m} \times 200$ μm shadow mask. MIS characterization was performed under ambient conditions using an Agilent B1500A semiconductor parameter analyzer.

Organic Thin-Film Transistor Fabrication and Electrical Characterization: Thermally deposited OTFTs. P5 and F₁₆CuPc films (40 nm thick) were deposited by thermal evaporation (deposition rate 0.1 Å s $^{-1}$) onto the PSAND- n coated substrates. The substrates were kept at 25 °C for P5 evaporation and at 125 °C for F₁₆CuPc evaporation. OTFT fabrication was completed by thermal evaporation (40 nm, 0.1–0.2 Å s $^{-1}$, base pressure $6\text{--}7 \times 10^{-6}$ Torr) of gold contacts ($W = 1500$ μm , $L = 150$ μm).

Solution-processed OTFTs. The DPP-DTT and PDIF-CN₂ films were deposited on PSAND- n coated substrates by spin-coating the corresponding solutions (4 mg mL $^{-1}$, CHCl_3) followed by thermal annealing at 200 °C for 20 min in an Argon filled glovebox. OTFT fabrication was completed by thermal evaporation (40 nm, 0.1–0.2 Å s $^{-1}$, base pressure $6\text{--}7 \times 10^{-6}$ Torr) of Au contacts ($W = 1500$ μm , $L = 150$ μm).

Flexible OTFT fabrication. The polyimide (PI, 25 μm thick) substrates were cleaned by ultrasonication in acetone and isopropyl alcohol and then subjected to an O_2 plasma for 10 min. Next, 3 nm Cr adhesion and 25 nm Au electrodes were subsequently thermal deposited on the PI using a shadow mask as gate electrode (0.1–0.2 Å s $^{-1}$, base pressure $6\text{--}7 \times 10^{-6}$ Torr). The dielectric and DPP-DTT films were fabricated using the aforementioned processes on the rigid substrates. Source-drain electrodes (30 nm-thick Au) were thermally evaporated through a metal shadow mask ($W = 1000$ μm , $L = 50$ μm).

OTFT electrical characterization. TFT electrical characterizations were performed under ambient conditions using an Agilent B1500A semiconductor parameter analyzer. The carrier mobility (μ) was measured in the saturation region with the conventional metal-oxide-semiconductor field-effect transistor model using Equation (4),^[38]

$$I_{\text{DS}} = \frac{\mu C_i W}{2L} (V_{\text{GS}} - V_{\text{TH}})^2 \quad (4)$$

where I_{DS} is the drain-source current, C_i is the dielectric capacitance per unit area of the PSAND, W and L are the channel width and length, respectively, V_{GS} is the gate-source voltage, and V_{TH} is the threshold voltage.

Blade-coated PSANDs. Blade-coated PSAND-1 were fabricated by first placing the substrate (n $^{++}$ -Si) on the blade-coater (Erichsen Coatmaster 510) setup with the surface maintained at a temperature of 50–70 °C. Next, the blade was approached the substrate maintaining a gap of 100–300 μm . After that, the precursor solution (20 μL for a 2 cm \times 2 cm square substrate) was placed at the interface between the substrate and the blade until a meniscus formed. For the growth of the ZrO_x primer layer, the precursor solution was identical to that used for the spin-coated

PSANDs. The blade was horizontally transported at a constant velocity of 10 mm s^{-1} . Finally, the film was annealed at 220°C for 20 min. For the linker deposition, the linker solution (4 mg mL^{-1} in CHCl_3) was bladed as the primer ZrO_x and the film annealed at 110°C for 20 min, followed by rinsing with CH_2Cl_2 twice. The P-PA was blade-coated using a 4 mg mL^{-1} CHCl_3 solution using the same blading conditions followed by annealing at 110°C for 20 min. Similar to the spin-coating process for PSANDs, the substrates were rinsed with CH_2Cl_2 . Finally, the ZrO_x capping layer was blade-coated using a 0.01 M ZrCl_4 solution in ethanol. The processing is identical to that of the ZrO_x primer. The HMDS-capped PSANDs films were fabricated by blade-coating (10 mm s^{-1}) pure HMDS on top of BC-PSAND-1 film, followed by annealing at 130°C for 20 min in ambient.

Characterization: The AFM images were recorded on a Bruker Dimensional Icon system in the tapping mode. XRR measurements were acquired with a Rigaku SmartLab diffraction workstation using $\text{Cu K}\alpha$ (1.54 \AA) radiation. NMR were recorded on Bruker Avance III HD system (500 MHz). UV-vis spectra were recorded on the Varian spectrometer. TGA-DSC characterizations were performed on the TG-600 with Argon flow of 70 mL min^{-1} , and the heating rate was $10^\circ\text{C min}^{-1}$.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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